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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/961,202	09/24/2001	Baruch Solomon	2207/12173	6536

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/961,202	SOLOMON ET AL.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *1-4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/24/01 & 11/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 5-10 should group with claims 11-25 into invention III in the response filed on September 24, 2004 is acknowledged.

Information Disclosure Statement

2. The Information Disclosure statement(s) field on 09/24/2001 and 11/15/2004 are both considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 5-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamashiroya (US PAT. 6,470,425).

Regarding claim 5, Yamashiroya disclosures a control method comprising on a cache hit, counting a number of accesses to a cache line that caused the hit, i.e., cache memory system comprising a hit/miss counter (300, figure 1) which counts the number of times a cache hit or miss occurs sequentially for each entry of the cache memory (col. 2 lines 33-40 and col. 2 line 44 through col. 3 line 8), if the count meets a predetermined threshold, enabling a segment builder, building and storing instruction segments from an output of the segment builder, i.e., cache memory system further comprising a hit threshold register (461, figure 3) wherein the hit threshold register contains number of sequential cache hits that is used as an update inhibition condition for a cache memory entry, and when the number of sequential cache hits on an entry exceeds the number of times specified in the hit threshold register, the update of the entry is inhibited thereafter (col. 3 line 50 through col. 4 line 53).

Regarding claim 6, Yamashiroya disclosures the control method further comprising if a hit also is registered in a segment cache, maintaining the segment builder disabled regardless of the count value (col. 4 lines 31-53).

Regarding claims 7-8, Yamashiroya disclosures the control method further comprising if a hit also is registered in a segment cache, maintaining the segment builder disabled regardless of the count value, and incrementing the count value and storing the incremented count value in the cache line (col. 3 line 45 through col. 4 line 53).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 9-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashiroya (US PAT. 6,470,425) in view of Chauvel et al. (US PAT. 6,681,297 hereinafter Chauvel).

Regarding claims 9-10, Yamashiroya differs from the claimed invention in not specifically teaches the control method further comprising identifying a victim cache line, and reducing a count value of the victim cache line, and identifying an age of cache lines in a same set as the cache line that caused the hit, and reducing a count value of those cache lines that are older than a median age of all the cache lines in the same set. However, Chanvel teaches in the cache memory system comprising a miss counter to count each cache memory request miss corresponding to a monitored-qualifier value, and further comparing with the miss rate threshold

to generate a flush command, and eviction the victim cache line based on a least recently use replacement algorithm (col. 13 line 61 through col. 14 line 63, col. 15 line 59 through col. 16 line 26 and col. 17 line 7 through col. 18 line 3). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the cache control method of Yamashiroya having steps of comprising identifying a victim cache line, and reducing a count value of the victim cache line, and identifying an age of cache lines in a same set as the cache line that caused the hit, and reducing a count value of those cache lines that are older than a median age of all the cache lines in the same set, as per teaching by the cache memory system of Chauvel, because it minimizes eviction of useful entries of active tasks and thereby reduces power consumption.

Regarding claim 11, Yamashiroya disclosures a cache comprising a plurality of entries (100, figure 1), each indexed comprising a tag field, a count field, i.e., hit /miss counter (300, figure 1) and a data field (200, figure 1), a incrementor (321 and 322, figure 2) coupled to the access count field, and a threshold comparator (417 and 472, figure 3) coupled to the incrementor via the hit/miss thresholds (461 and 462, figure 3) and (col. 2 line 10 through col. 3 line 8 and col. 3 line 50 through col. 4 line 50). Although Yamashiroya does not clearly disclosures the cache memory further comprising an address decoder and each indexed is output by the address decoder, Yamashiroya teaches each of the entry is output by the processor via the address register (10, figure 1), thus, it is well know in the art at the time the invention was made to recognize that processor is included instruction decoder/encoder to decode/encode the requested instruction to perform cache control operation in response to executing certain instructions which may include parameters to specify the requested operation, as an example of a

statement in Chanvel (col. 15 lines 45-54). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the cache memory of Yaashiroya in having an address decoder and each indexed is output by the address decoder, as per teaching by Chanvel, because it minimizes eviction of useful entries of active tasks and thereby reduces power consumption.

Regarding claim 12, Yamashiroya disclosures the cache further comprising a tag comparator (20, figure 1) coupled to the tag fields via bus (101, figure 1), a transmission gate coupled to the incrementor and controlled by and output from the tag comparator (figure 2).

Regarding claim 13, Yamashiroya disclosures write control logic (400, figure 1) controlled by an output of the tag comparator (col. 3 line 46 through col. 4 line 40).

Regarding claims 14-15, the limitations of the claims are rejected as the same reasons set forth in claims 9-10.

Regarding claim 16, the limitations of the claim are rejected as the same reasons set forth in claim 11.

Regarding claim 17, the limitations of the claim are rejected as the same reasons set forth in claim 12.

Regarding claims 18-19, the limitations of the claims are rejected as the same reasons set forth in claims 9-10.

Regarding claim 20, the limitations of the claim are rejected as the same reasons set forth in claim 13.

Regarding claim 21, Yamashiroya disclosures an access filter comprising a plurality of entries, each comprising a tag field (100, figure 1), a tag comparator (20, figure 1) coupled to the

tag field (figure 1 and col. 2 lines 9-32). Although Yamashiroya does not clearly disclosures the cache memory further comprising an address decoder and each indexed is output by the address decoder, Yamashiroya teaches each of the entry is output by the processor via the address register (10, figure 1), thus, it is well know in the art at the time the invention was made to recognize that processor is included instruction decoder/encoder to decode/encode the requested instruction to perform cache control operation in response to executing certain instructions which may include parameters to specify the requested operation, as an example of a statement in Chanvel (col. 15 lines 45-54). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the access filter of Yaashiroya in having an address decoder and each indexed is output by the address decoder, as per teaching by Chanvel, because it minimizes eviction of useful entries of active tasks and thereby reduces power consumption.

Regarding claim 22, Yamashiroya disclosures the access filter further comprising a count field, i.e., hit/miss counter (300, figure 1), provided within each of the entries (col. 2 line 33 through col. 3 line 8), an incrementor (311, figure 2) coupled to the count fields (figure 2), and a threshold comparator coupled to the incrementor, i.e., (417 and 472, figure 3) coupled to the incrementor via the hit/miss thresholds (461 and 462, figure 3) and (col. 2 line 10 through col. 3 line 8 and col. 3 line 50 through col. 4 line 50).

Regarding claim 23, Yamashiroya disclosures the access filter further comprising a count field provided within each of the entries, a threshold comparator coupled to the count fields, and an incrementor coupled to the incrementor (figures 1-2 and col. 2 line 33 through col. 3 line 8 and col. 3 line 50 through col. 4 line 53).

Regarding claim 24, Yamashiroya disclosures the access filter further comprising a write controller (400, figure 1) coupled to an output of the incrementor (col. 3 line 33 through col. 4 line 39).

Regarding claim 25, Yamashiroya disclosures the access filter comprising an output of the tag compartaor enables a segment builder (col. 3 line 33 through col. 4 line 53).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bruce et al. (US PAT. 6,000,006) disclosures unified re-map and cache-index table with dual write-counters for wear-leveling of non-volatile flash ram mass storage (abstract).

Pardo et al. (US PAT. 5,586,279) disclosures data processing system and method for testing a data processor having a cache memory (col. 2 lines 9-58).

Iacobovici et al. (US PAT. 5,860,095) disclosures conflict cache having cache mis-counters for a computer memory system (abstract).

Bryan Black et al. *The Block-based Trace Cache* under Department of Electrical and Computer Engineering Carnegie Mellon University at Pittsburgh, published in 1999 (abstract)

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tue-Fri 8:30 a.m. to 6:00 p.m.:

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo Li

Patent Examiner
Art Unit 2186

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